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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/069,517	03/05/2002	Claude Jaussaud	220040US2PCT	9383
22850	7590	09/21/2004	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.			GUERRERO, MARIA F	
1940 DUKE STREET			ART UNIT	
ALEXANDRIA, VA 22314			PAPER NUMBER	
			2822	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/069,517

Applicant(s)

JAUSSAUD ET AL.

Examiner

Maria Guerrero

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 September 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 11-13 and 16-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 11-13 and 16-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This Office Action is in response to the Amendment and the Request for continued examination filed September 3, 2004.

Status of Claims

2. Claims 1-10 and 14-15 are canceled. Claims 11-13 and 16-21 are pending.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 3, 2004 has been entered.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 11, 13, 16, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Linn et al. (U.S. 5,387,555).

6. Linn et al. teaches a method of creating an electrically conducting bonding between a face of a first semiconductor element and face of a second semiconductor element by heat treatment (col. 4, lines 1-15). Linn et al. discloses depositing at least one layer of material on the face of the first semiconductor element and at least one layer of material on the face of the second semiconductor element (Fig. 3a, 5a, col. 3, lines 49-56). Linn et al. teaches combining the layers to form a layer that provides electrically conducting bonding between the two faces (Fig. 3b, Fig. 5b, col. 3, lines 56-65, col. 4, lines 5-15). Linn et al. shows applying the first and second faces one against the other and carrying out a heat treatment (Fig. 3b, 5b, col. 3, lines 55-65). Linn et al. teaches reacting the layers of material to form a temperature stable mixture with respect to the first and second semiconductor elements (col. 3, lines 55-68, col. 5, lines 35-67, col. 6, lines 1-6). Linn et al. discloses not inducing any reaction product between the deposited layer of material and at least one of the semiconductor elements during the heat treatment (Fig. 4a-4b, col. 5, lines 35-67). Linn et al. teaches forming at least one oxide layer onto at least one of the deposited conductive layers and the oxide reacts such that the oxide formed is in a form of isolated precipitates that do not substantially harm the electrically conducting bonding (Fig. 5a-5b, col. 6, lines 58-67, col. 7, lines 1-28).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 12 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Linn et al. (U.S. 5,387,555) in view of Goesele et al. (U.S. 5,877,070).

Linn et al. also teaches the interposed layers comprising a layer of tungsten and a layer of silicon that could be on one of or both faces (col. 8, lines 20-25). Linn et al. teaches forming WSi₂ during the heat treatment (Fig. 5b, col. 7, lines 3-15).

Regarding claim 17, Linn et al. does not specifically show the first and second semiconductor elements being SiC. However, Goesele et al. shows the use of SiC in the bonding process as conventional in the art (col. 3, lines 50-60, col. 6, lines 15-16).

Regarding claims 12 and 18-20, Linn et al. does not specifically show the preliminary step of forming a thin film by forming microcavities on a substrate by ionic implantation. However, Goesele et al. teaches forming the thin film on the substrate by forming microcavities using ionic implantation (col. 6, lines 15-20, col. 10, lines 13-30).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Linn et al. reference by including the steps of forming the thin film on the substrate by forming microcavities using ionic implantation and using

SIC as taught Goesele et al. in order to increase device performance and thermal stability.

Response to Arguments

8. Applicant's arguments filed September 3, 2004 have been fully considered but they are not persuasive. Claims 11-13 and 16-21 stand rejected.

Applicant argued that Linn et al. does not disclose directly depositing on the face of the first and second semiconductor because there is an electrically insulating material interposed between the semiconductor elements. However, Linn et al. discloses depositing at least one layer of material on the face of the first semiconductor element and at least one layer of material on the face of the second semiconductor element (Fig. 3a, 5a, col. 3, lines 49-56). Linn et al. teaches combining the layers to form a layer that provides electrically conducting bonding between the two faces (Fig. 3b, Fig. 5b, col. 3, lines 56-65, col. 4, lines 5-15). Linn anticipates the claims because the presence of the electrically insulating material does not constituted a teaching away. Linn et al. teaches combining the layers to form a layer that provides electrically conducting bonding between the semiconductors faces (Fig. 3a-3b, 4a-44b).

Applicant argued that the applied art is completely silent as to how to achieve an electrical conducting bonding layer between two semiconductor elements. However, a person of ordinary skill would recognize that Linn shows providing and electrically conducting bonding between the two faces of the semiconductor elements (Fig. 3a-3b, 4a-6, Abstract).

In addition, the elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

Furthermore, during patent examination, the pending claims must be “given *>their< broadest reasonable interpretation consistent with the specification.” > In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). While the claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allow. > In re American Academy of Science Tech Center, F.3d , 2004 WL 1067528 (Fed. Cir. May 13, 2004)(The USPTO uses a different standard for construing claims than that used by district courts; during examination the USPTO must give claims their broadest reasonable interpretation.) < This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) >; Chef America, Inc. v. Lamb-Weston, Inc., 358 F.3d 1371, 1372, 69 USPQ2d 1857 (Fed. Cir. 2004).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cantarini et al. (U.S. 5,973,257) is cited as evidence to show that

Art Unit: 2822


the bonding layer formed by Linn is recognize in the art as an electrical conducting bonding layer (Cantarini et al., col. 4, lines 34-37).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maria Guerrero whose telephone number is 571-272-1837.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

September 17, 2004


MARIA F. GUERRERO
PRIMARY EXAMINER